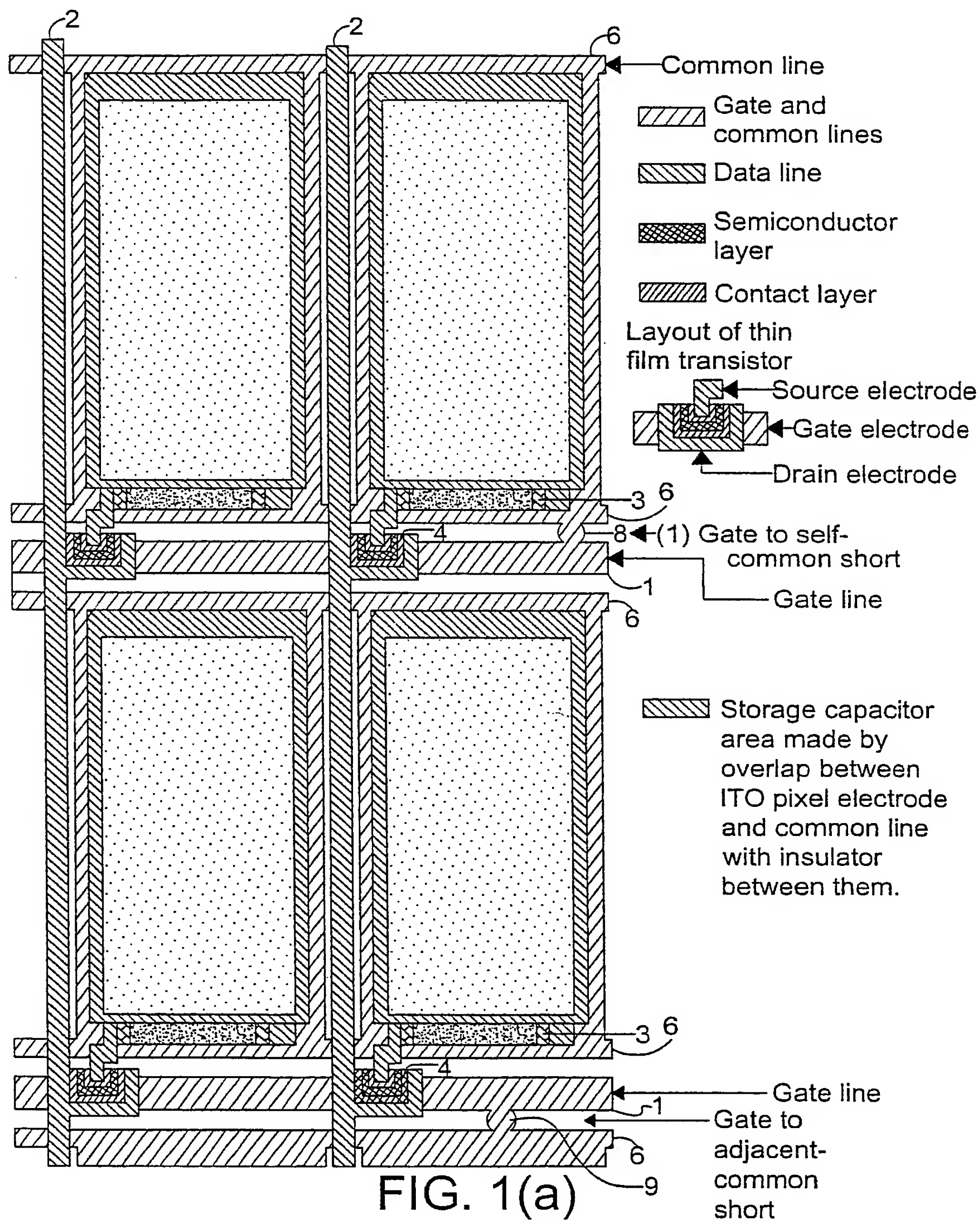Gate to common short defects in TFT array with double common line layout.

FIG. 1(a)

Explanation of pixel layout by showing four pixels in different process step.
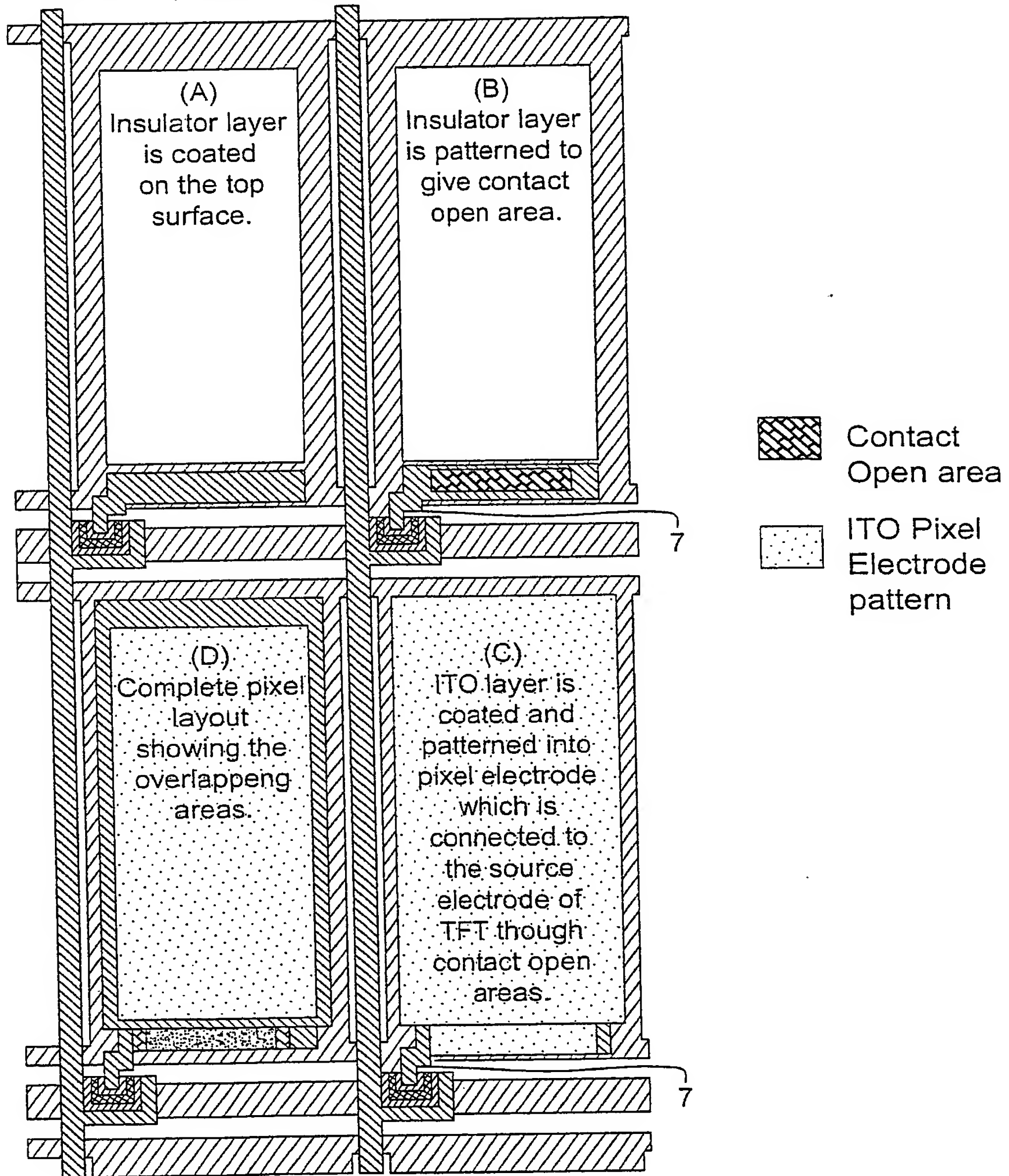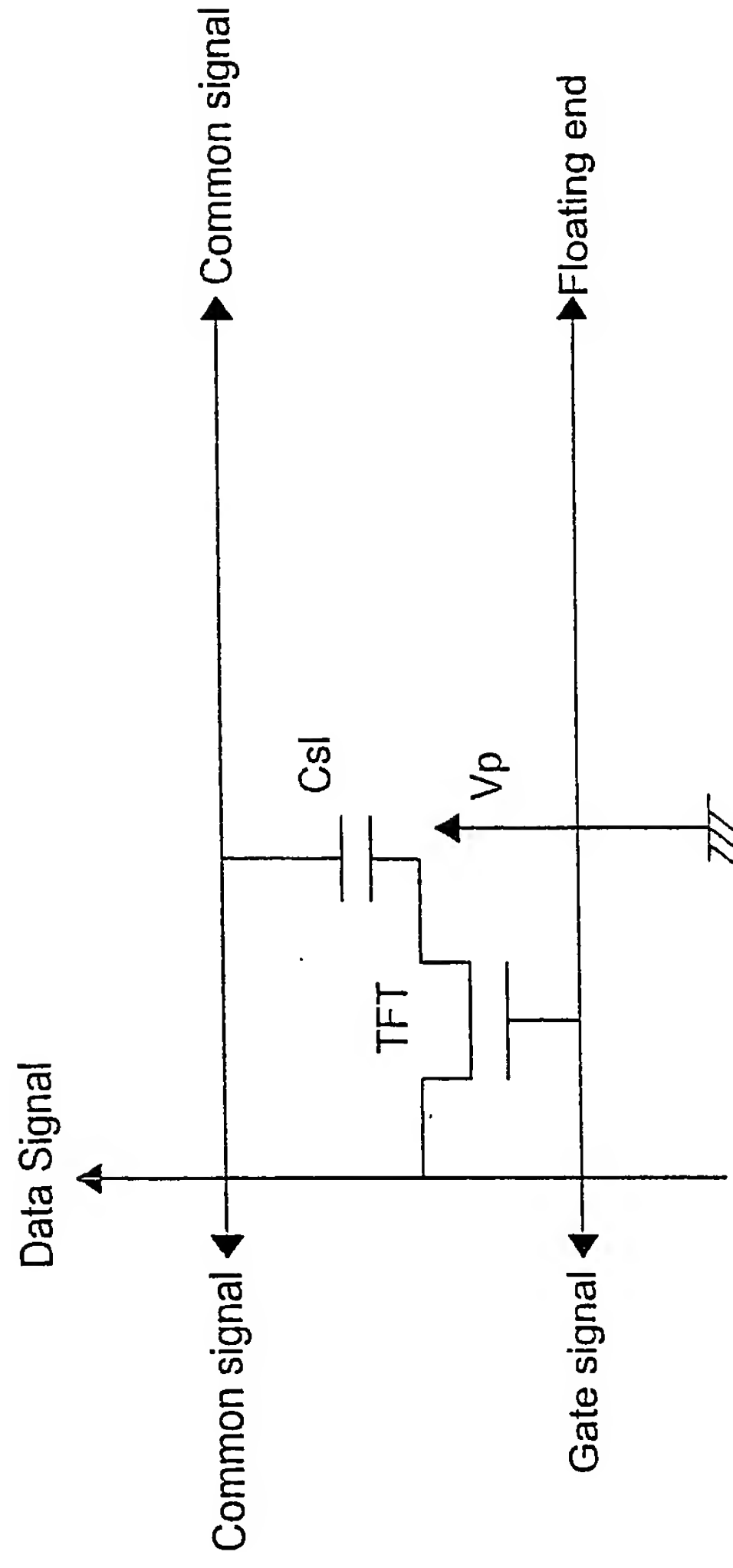

(A)
Insulator layer is coated on the top surface.

(B)
Insulator layer is patterned to give contact open area.

(D)
Complete pixel layout showing the overlappeng areas.

(C)
ITO layer is coated and patterned into pixel electrode which is connected to the source electrode of TFT though contact open areas.

7

7

Contact Open area

ITO Pixel Electrode pattern

FIG. 1(b)

FIG. 2

Simplified equivalent circuit of one cross point in TFT array

Applying a Test Signal
to the TFT Array ⟋10

Monitoring Pixel Voltages
Along Gate Line ⟋20

Detecting a Defect Along Gate
Line Based on Pixel Voltage
Variations ⟋30

Determining Location of defect
by Analyzing Pixel
Voltage Profile ⟋40

Correcting the Defect ⟋50
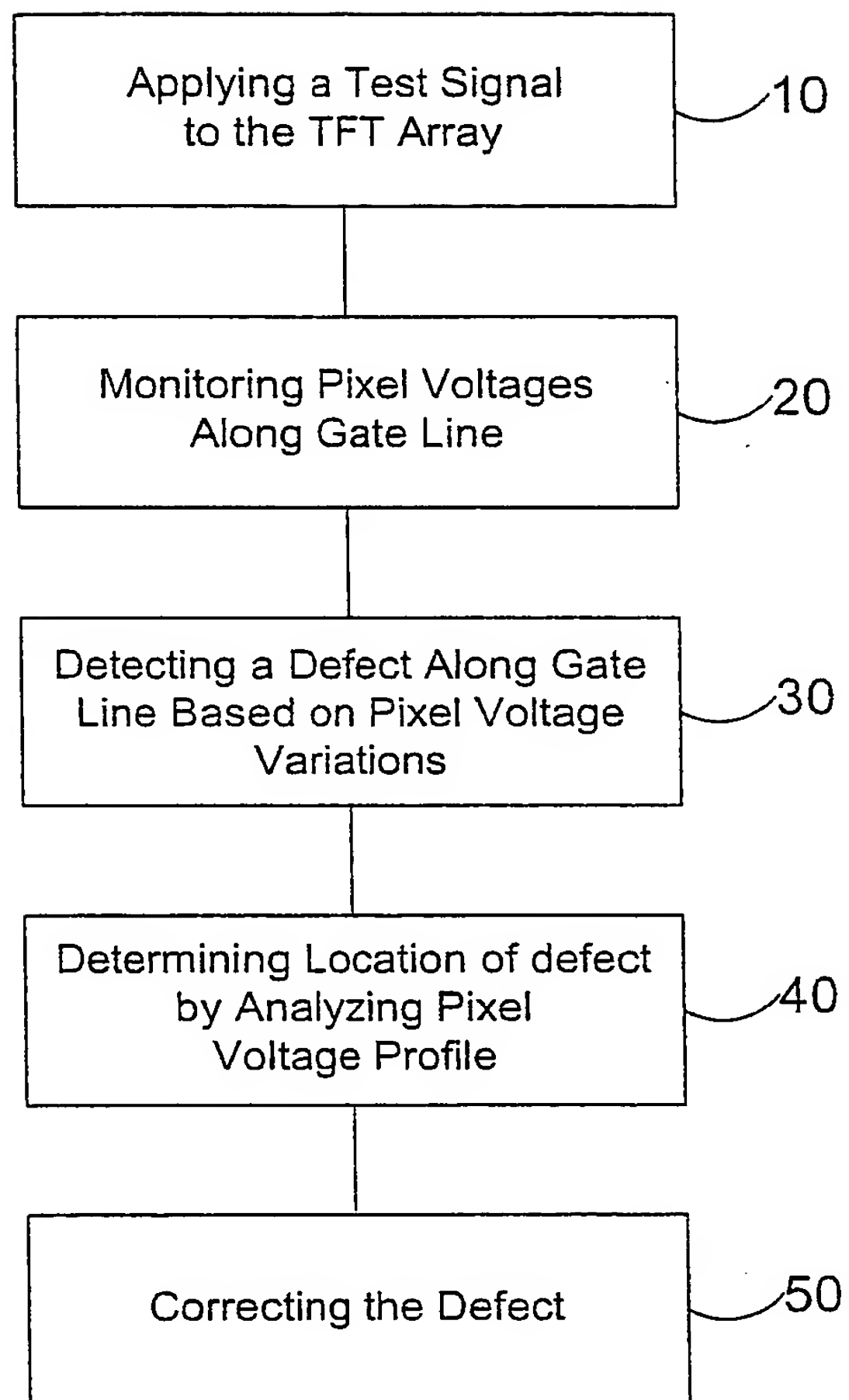
FIG. 3

Signal patterns to detect the short defect between gate and common lines.
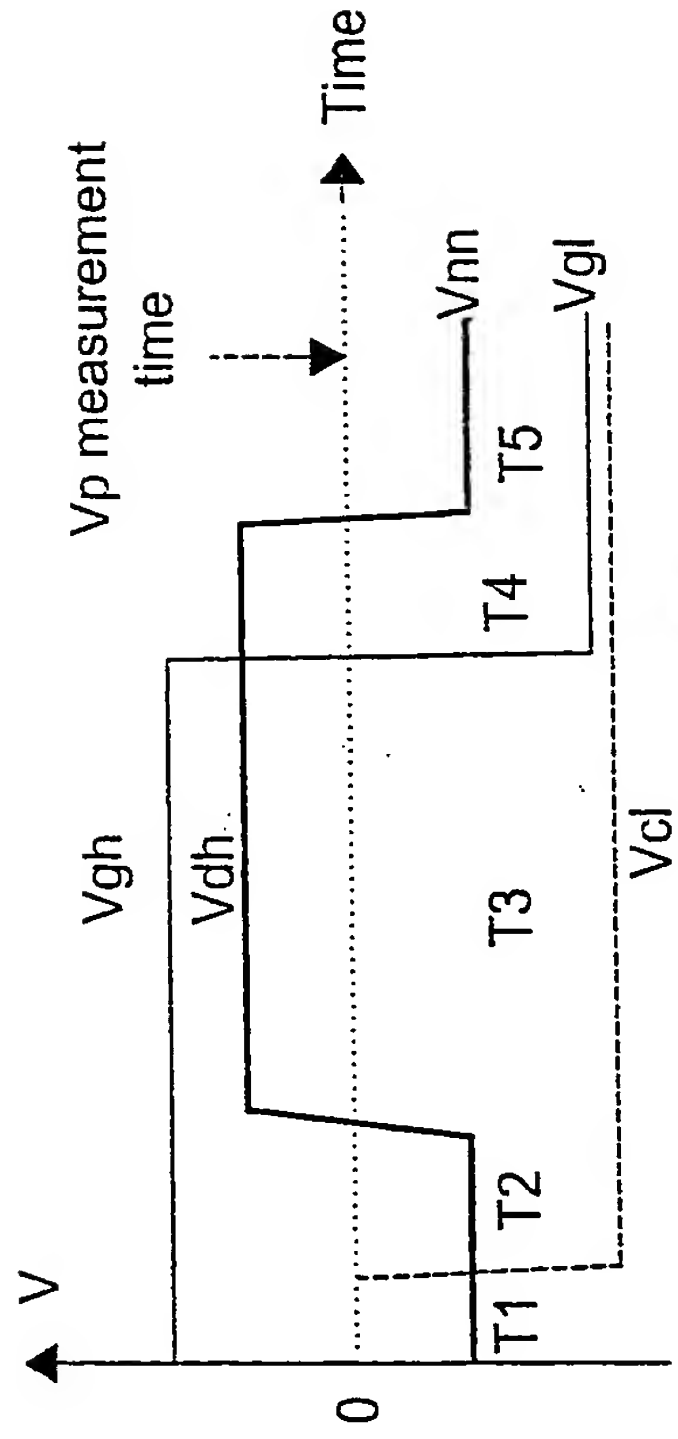
FIG. 4(a)

Signal patterns for positive pixel voltage

Gate signal
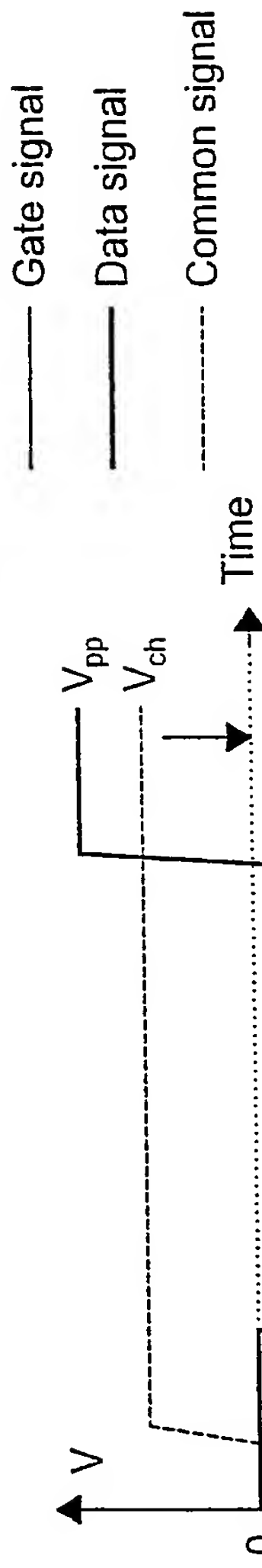Data signal
Common signal

FIG. 4(b)

Signal patterns for negative pixel voltage

Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of Fig. 4 (a) is applied.
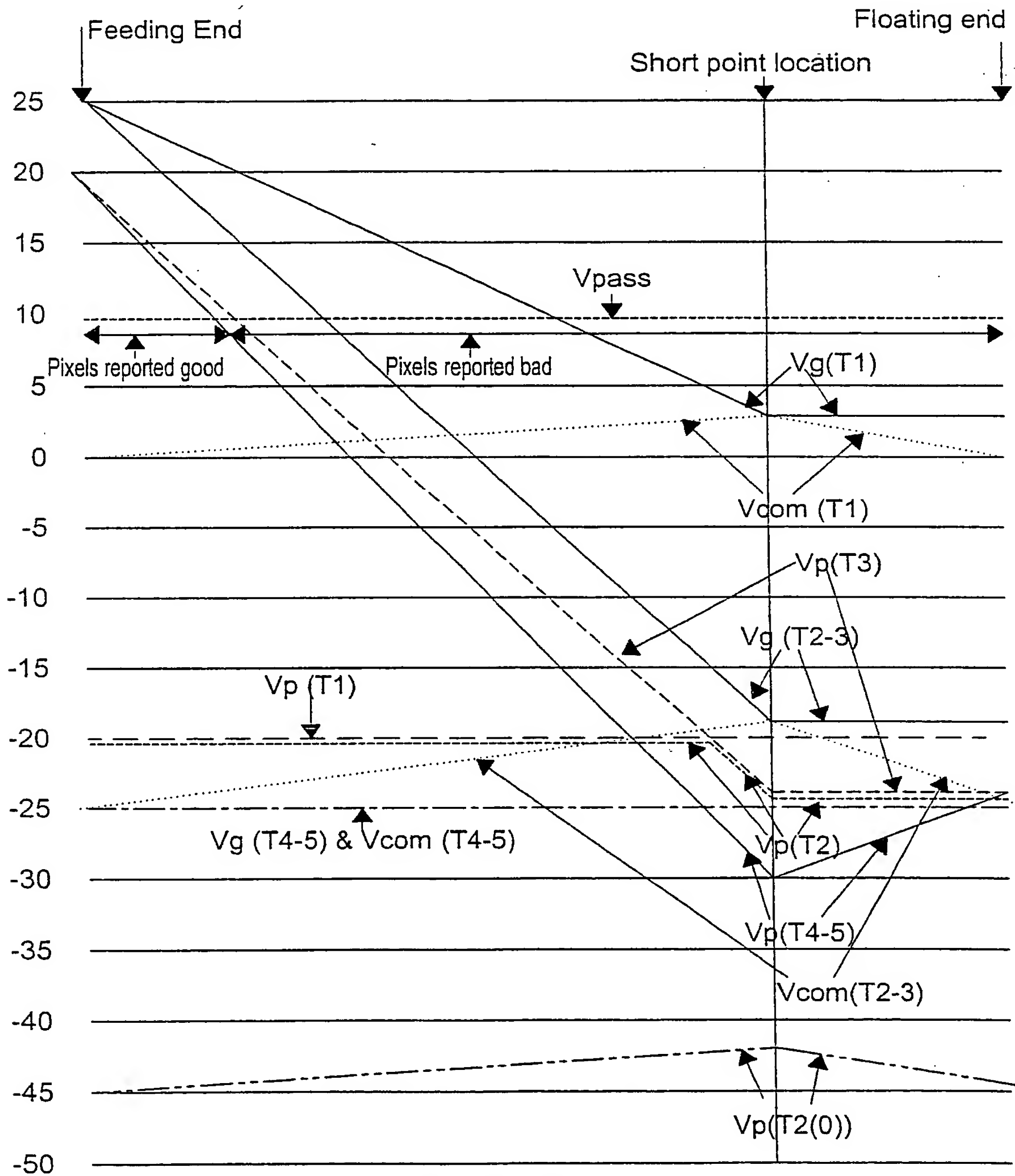

FIG. 5

Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of FIG. 4 (b) is applied.
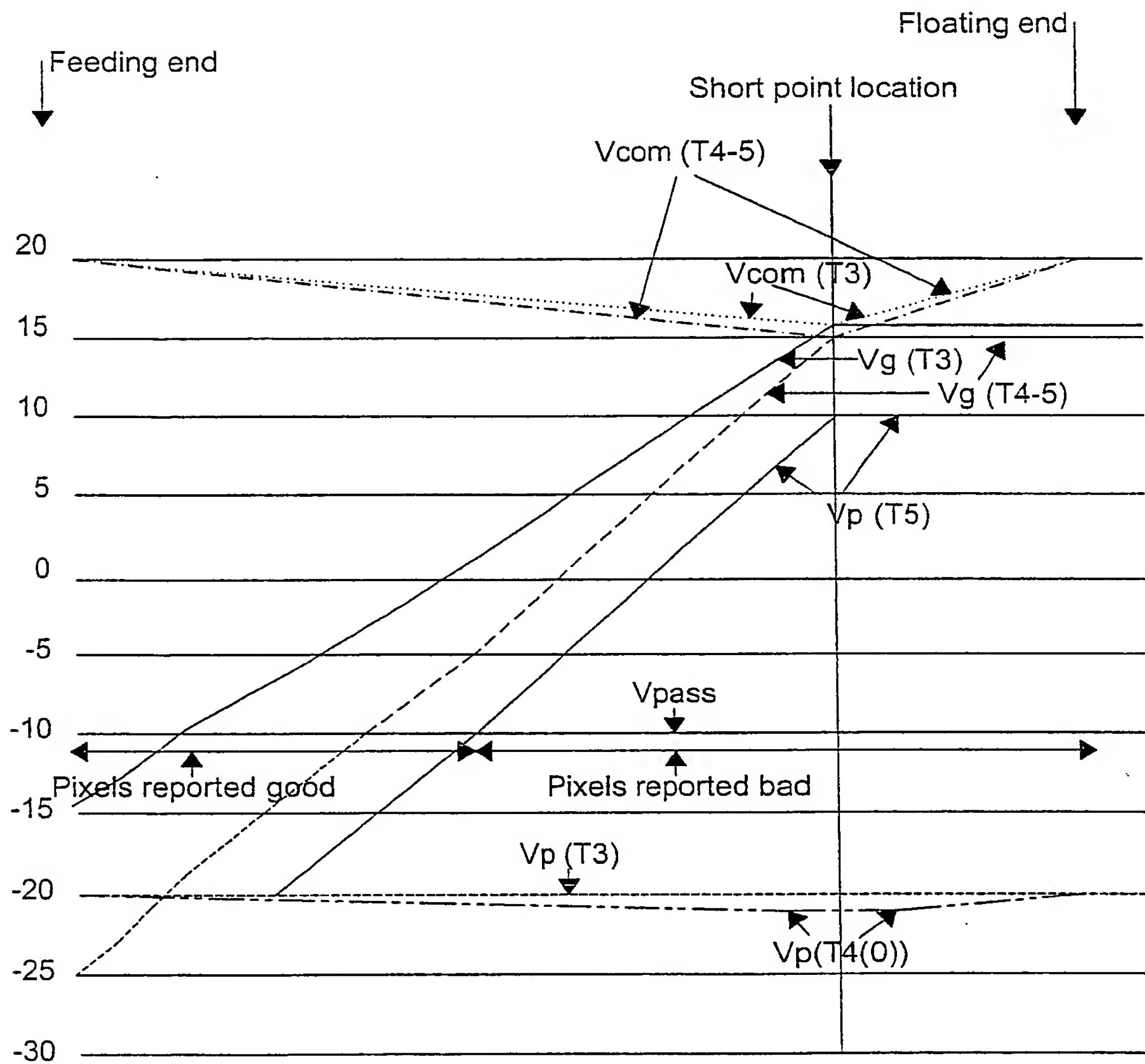

FIG. 6

Calculation of pixel voltages (Vp (T4-5) of Fig. 5 - Vp (T5) of Fig. 6) along the gate line with a short defect between gate and self-common lines.

FIG. 7

Analysis of pixel voltages along the gate line with a short
defect between gate and adjacent-common lines when the signal
patterns of Fig. 4 (a) is applied.

Feeding end

Short point location

Floating end

25

Vp_aj (T3)

20

15

Vpass

Vp_aj (T4-5)

10

Pixels reported good   Pixels reported bad

Vg (T1)

5

0

Vcom_aj (T1)

-5

Vp (T3-5)

-10

Vg (T2-3)

-15

Vp_aj (T2)   Vp (T1) & Vp_aj (T1)

-20

-25

Vg (T4-5) & Vcom_aj (T4-5)   Vp (T2)

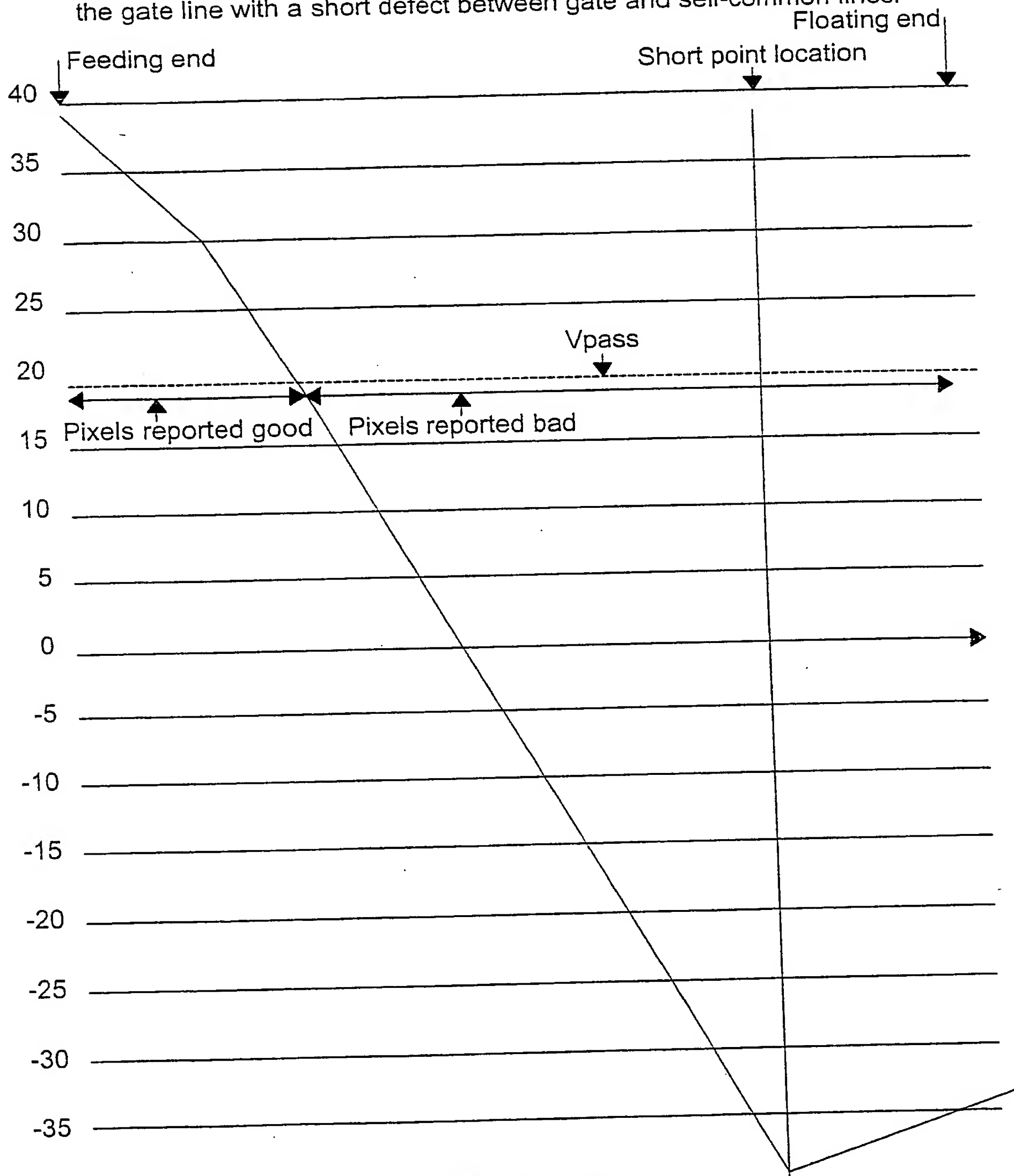-30

Vcom_aj (T2-3)

-35

Vp_aj (T2(0))

-40

-45

Vp (T2(0))

FIG. 8

Analysis of pixel voltages along the gate line with a short defect between
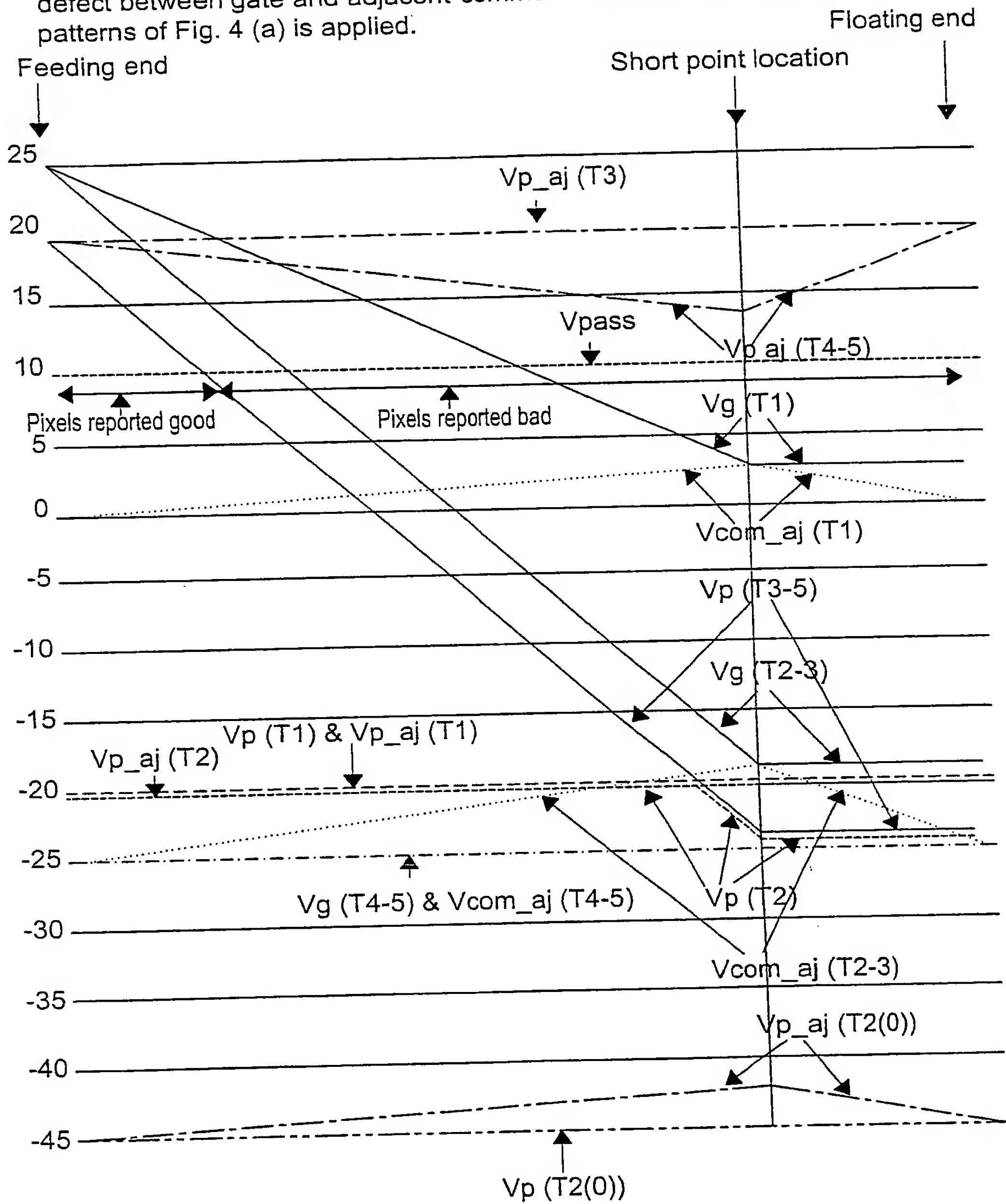gate and adjacent-common lines when the signal patterns of FIG. 4 (b) is applied.
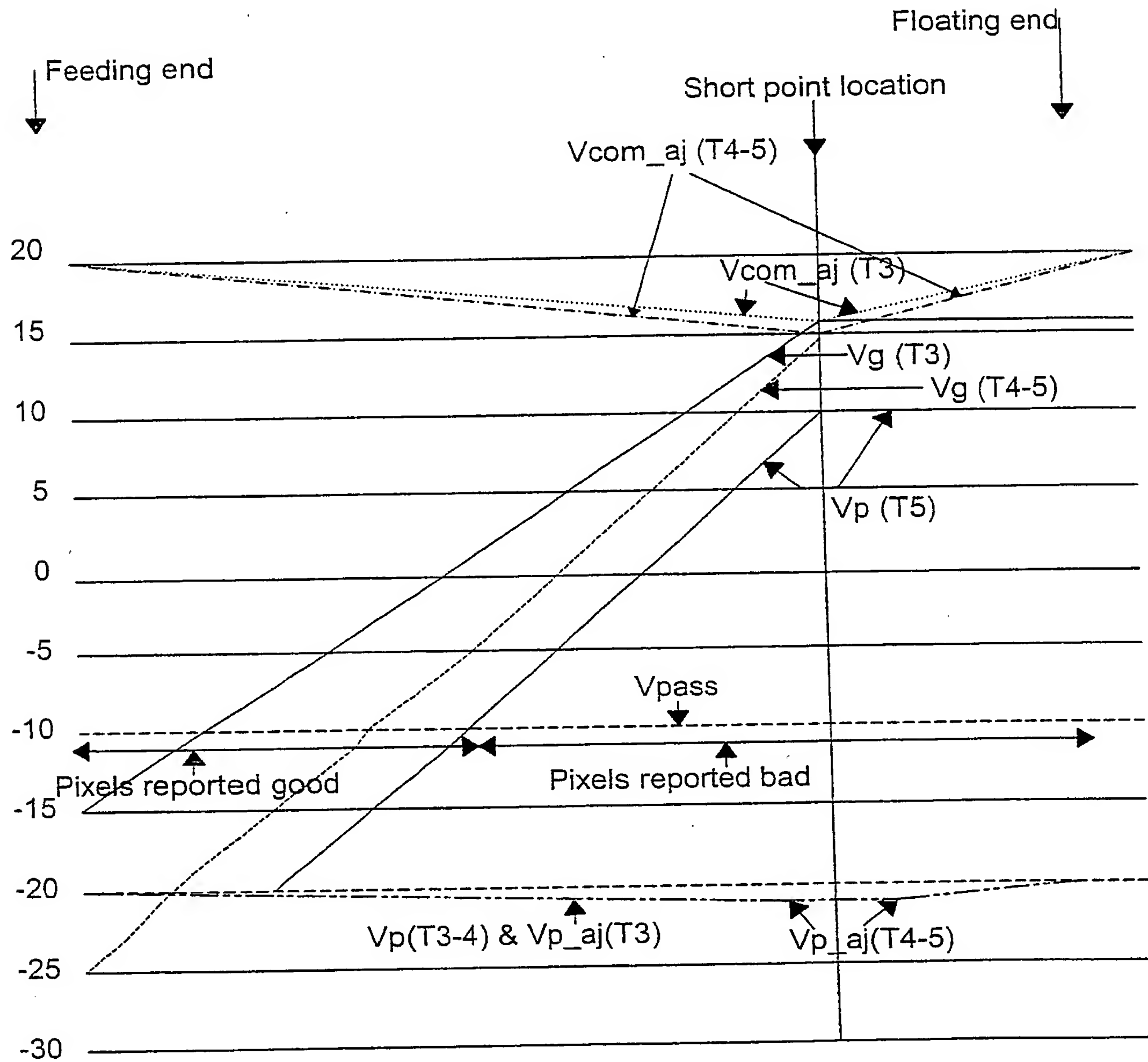

FIG. 9

Calculation of pixel voltages (Vp (T3-5) of Fig 8-Vp (T5) of Fig 9) along
the gate line with a short defect between gate and adjacent-common lines.

FIG. 10

FIG. 11

Applying a Test Signal to a Circuit — 200

Obtaining a Response Signal — 210

Comparing the Response Signal to Reference Information — 220

Classifying a Circuit Defect Based on the Comparison — 230

Identifying a Manufacturing Process Problem Based on Classified Defect — 240

Adjusting the Process to Correct the Problem — 250
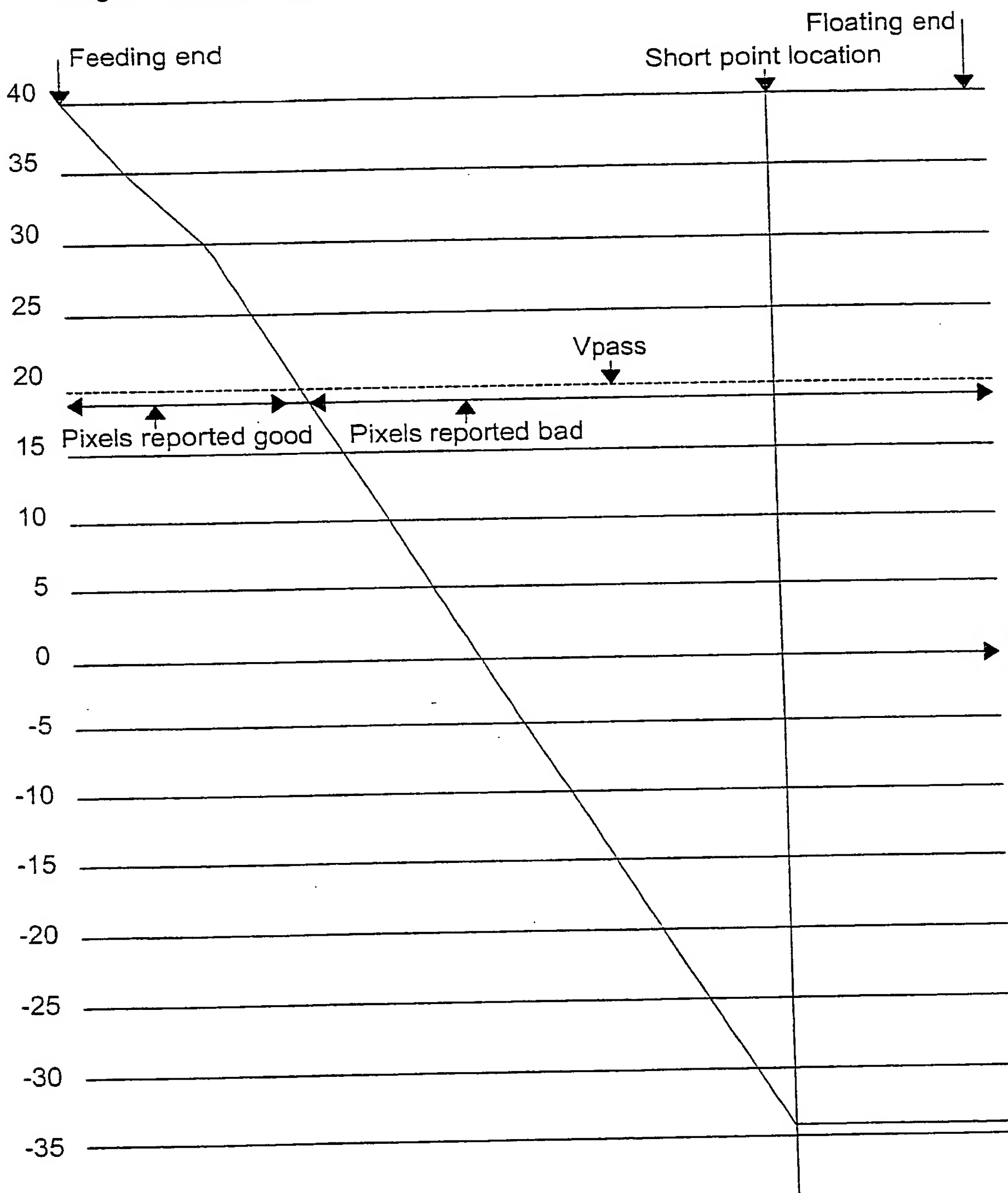
FIG. 12

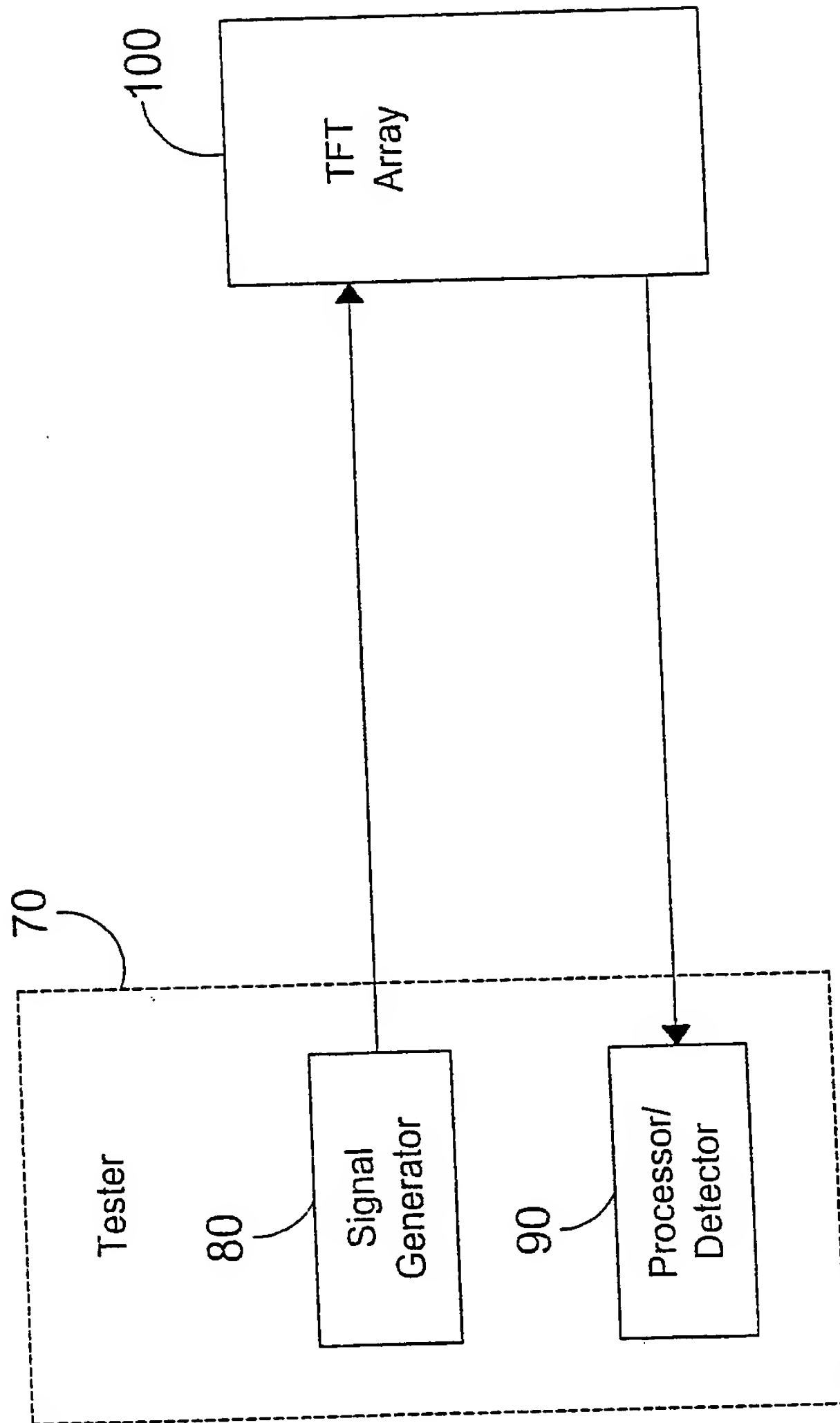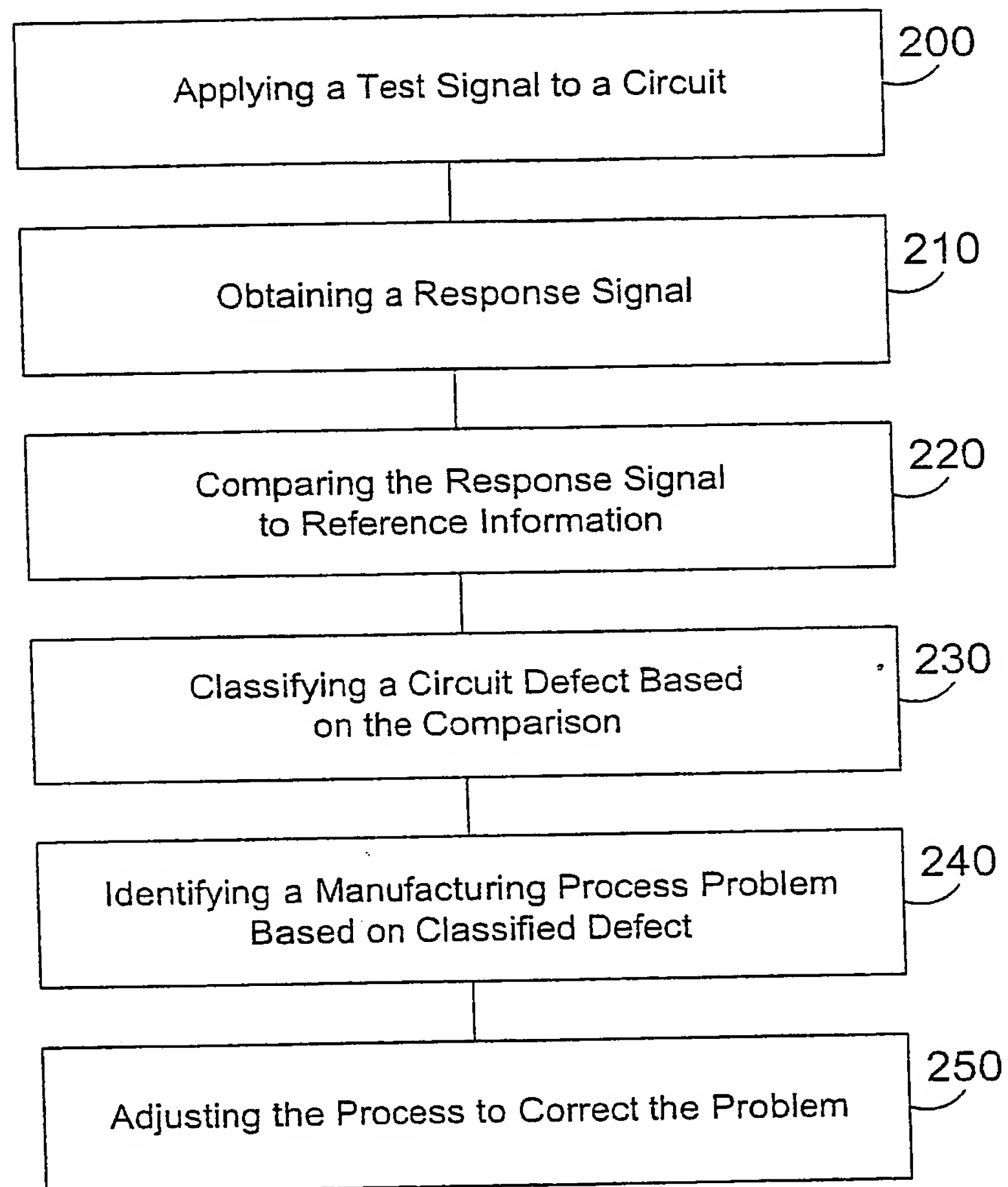Defect Histogram that was obtained using ideal distribution of defect signals for defects d1, d2, and dn, where Vd1, Vd2, and Vdn are the representative defect signals for d1, d2 and dn, respectively, and the defect signal zones for the defects d1, d2 and dn.
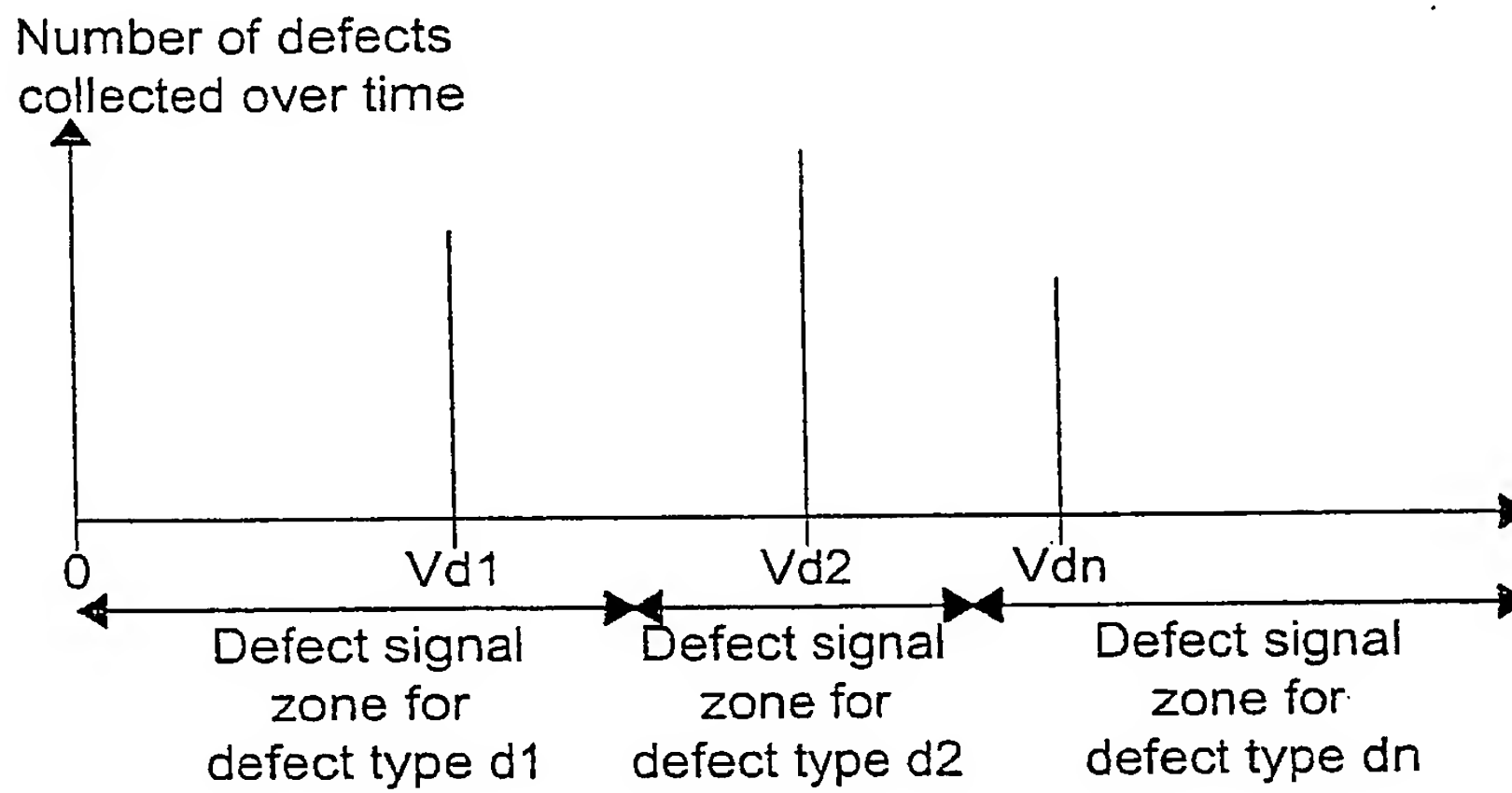
FIG. 13

Realistic distribution of the defect signals for the defects d1, d2 and dn, where normal distribution function is used for each defect type.
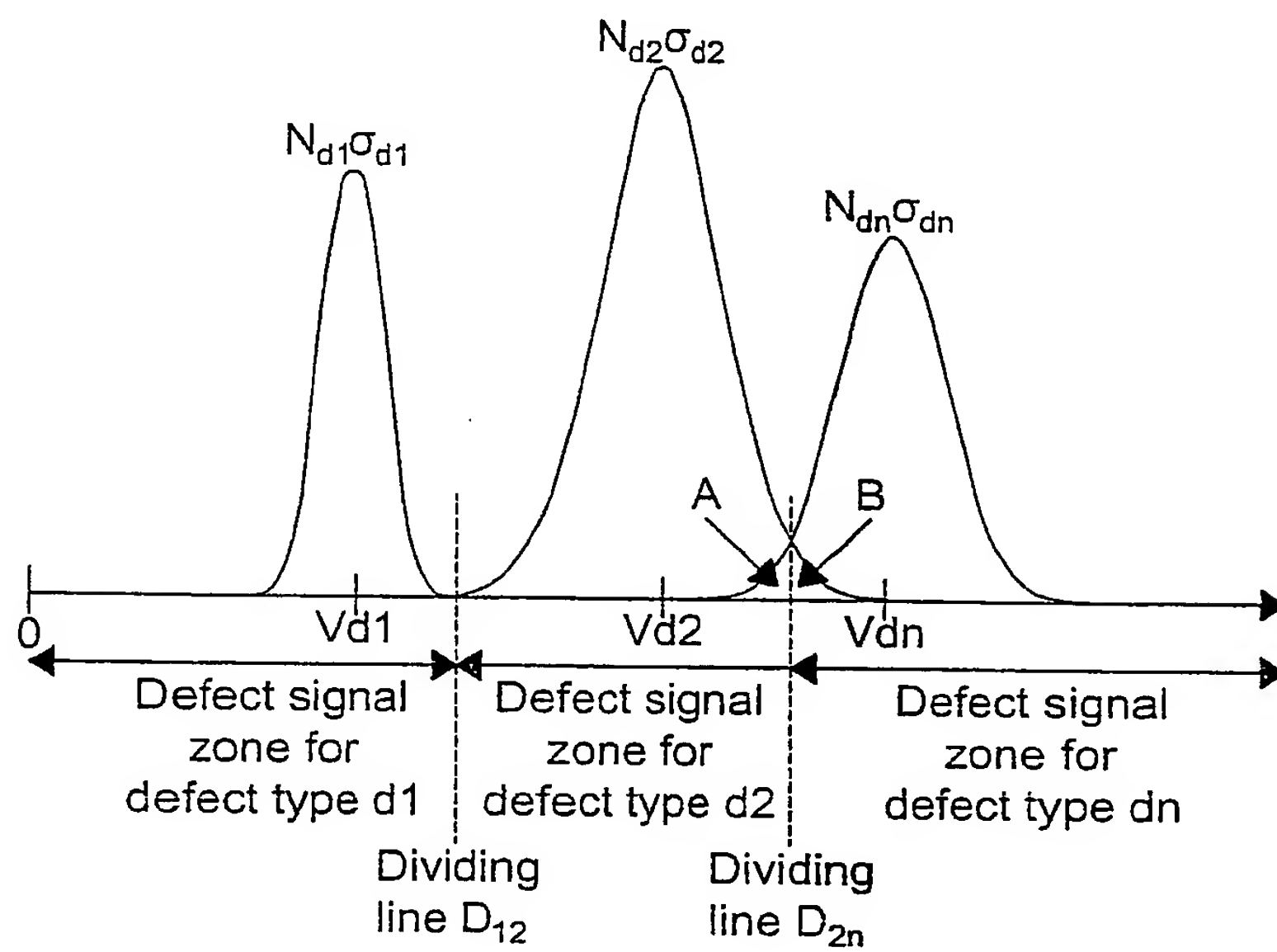
Defect signal

FIG. 14

Explanation of pixel layout by showing four pixels in different process step.

(A)
Passivation insulator layer is coated on the top surface.

(B)
Passivation insulator layer is patterned to give contact open via area.

(D)
Complete pixel layout showing the overlapped areas.

(C)
ITO layer is coated and patterned into pixel electrode which is connected to the source electrode of TFT through contact open area.

Mask #1
Gate and common lines

Mask #2
Semiconductor layer
Contact layer

Mask #3
Data line

Mask #4
Contact Open area

Mask #5
ITO Pixel Electrode area

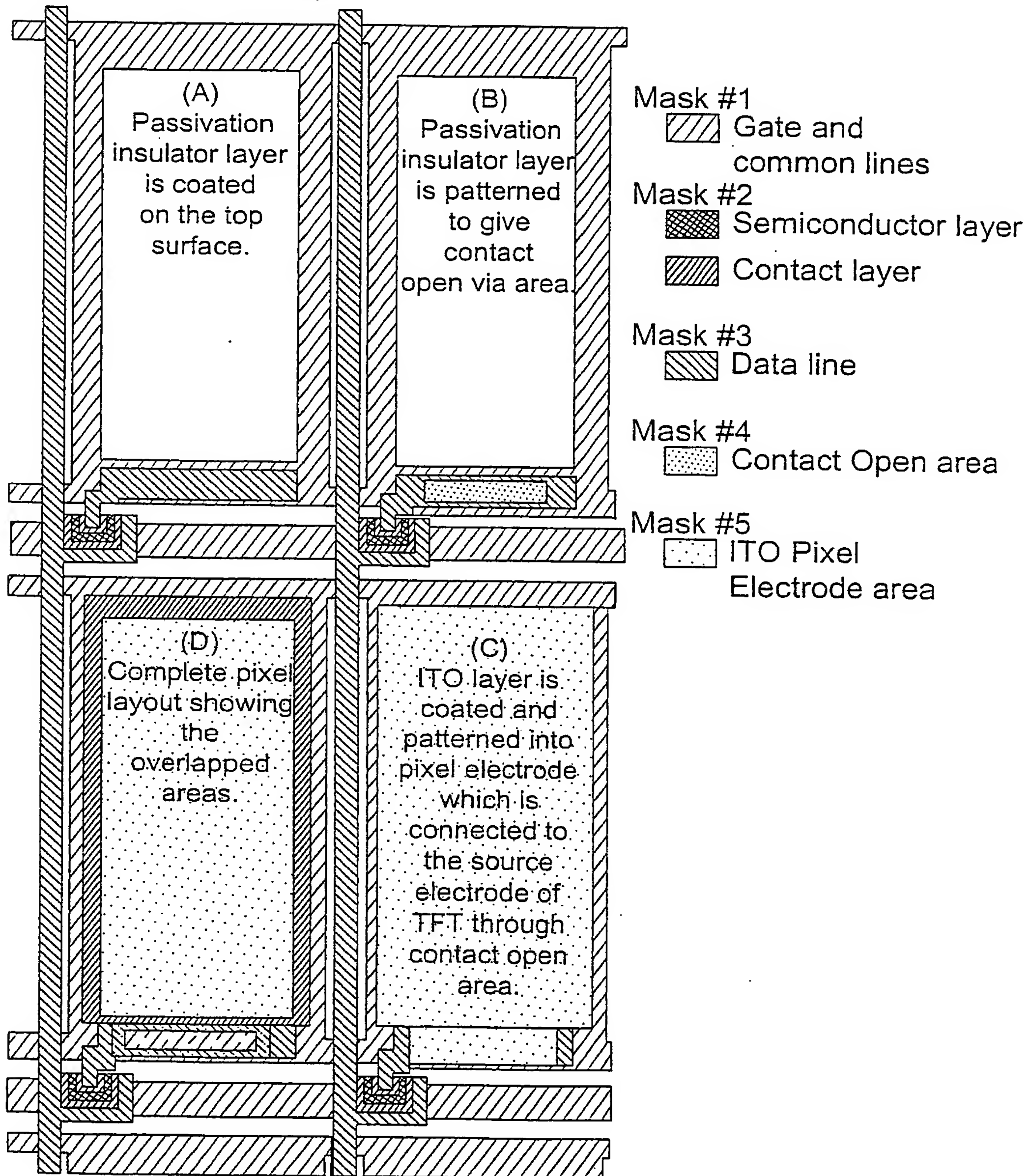FIG. 15

Example of the process flow for TFT-array

| Deposition and patterning (by mask #1) of gate and common lines | —300 |

↓

| Deposition of gate insulator | —310 |

↓

| Deposition and patterning (by mask #2) of semiconductor and contact layers together | —320 |

↓

| Deposition and patterning (by mask #3) of data lines | —330 |

↓

| Etching of contact layer using data line as etch-blocking layer | —340 |

↓

| Deposition of passivation insulator | —350 |

↓

| Opening of via area using mask #4 | —360 |

↓

| Deposition and patterning (by mask #5) of ITO pixel electrode | —370 |

FIG. 16